CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent are:

1. A method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of:

forming a graded $Si_{1-x}Ge_x$ epitaxial layer on a first single crystalline semiconductor substrate,

forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer over said graded $Si_{1-x}Ge_x$ layer,

smoothing the surface of said relaxed $Si_{1-y}Ge_y$ epitaxial layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS),

selecting a second substrate, said second substrate with or without an insulator having a major surface with a surface roughness in the range from about 0.3 nm to about 1 nm RMS,

bonding said top surface of said relaxed $Si_{1-y}Ge_y$ epitaxial layer on said first substrate to the top surface of said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a single mechanical structure.

2. The method of claim 1 further including the step of smoothing the upper surface of said relaxed $Si_{1-y}Ge_y$ layer on said second substrate whereby additional epitaxial layers may be grown.

3. The method of claim 2 further including the step of growing an epitaxial layer of a material selected from the group consisting of $Si_{1-y}Ge_y$, Si, SiC, Ge, GeC, and $Si_{1-y}Ge_yC$.

4. The method of claim 3 wherein said $Si_{1-y}Ge_y$ material is selected with a value of y to provide a strained layer or to reduce the bandgap of SiGe to allow absorption of light in the infrared range (>1um in wavelength).

5. The method of claim 1 further including the step of removing said first substrate.

6. The method of claim 1 wherein said low-defect relaxed $Si_{1-y}Ge_y$ layer on said second substrate has a thickness in the range from about 50nm to about 1000nm as determined by the layer structure formed on said first substrate.

7. The method of claim 1 wherein an encapsulation layer of a material selected from the group consisting of Si, SiO_2, Poly Si, and Si_3N_4 is formed on the surface of said relaxed SiGe layer of said first substrate.

8. The method of claim 7 wherein said encapsulation layer is formed and annealed at a temperature in the range from about 400°C to about 900°C.

9. The method of claim 1 wherein said first substrate is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, or InP.

10. The method of claim 1 wherein said said step of smoothing further includes the step of Chemical-Mechanical Planarization (CMP) to smooth said surface of said relaxed $Si_{1-y}Ge_y$ layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm RMS.

11. The method of claim 1 wherein after said step of forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer further includes the step of forming an encapsulation layer.

12. The method of claim 11 wherein said said step of smoothing further includes the step of Chemical-Mechanical Planarization (CMP) to smooth the surface of said encapsulation layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm RMS.

13. The method of claim 1 wherein an insulator layer is formed on said second substrate for the formation of strained Si/SiGe on insulator and a conducting layer is formed on said second substrate for the formation of p-i-n SiGe/Si heterodiodes.

14. The method of claim 13 wherein said insulator layer includes a material selected from the group consisting of SiO_2, Si_3N_4, Al_2O_3, $LiNbO_3$, low-k materials where k is less than 3.2, or the combination of two or more said materials.

15. The method of claim 13 wherein said conducting layer includes heavily doped p+ Si or p+ Poly Si.

16. The method of claim 13 wherein said insulator layer is formed by a process selected from the group consisting of PECVD, LPCVD, UHVCVD and spin-on techniques.

17. The method of claim 13 wherein said insulator layer is formed at a temperature in the range from about 400°C to about 900°C.

18. The method of claim 1 wherein said second substrate is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, InP, sapphire, glass, quartz, $LiNbO_3$, and PLZT.

19. The method of claim 1 wherein said smoothed top surface of said first $Si_{1-y}Ge_y$ relaxed layer on said first substrate is brought into intimate contact with said top surface of an insulator layer on said second substrate.

20. The method of claim 18 wherein an intermediate agent layer selected from the group consisting of Ge, Al, W, Co, and Ti may be used to enhance the bonding interface.

21. The method of claim 1 wherein said step of annealing includes thermal treatment cycles to form a strong bond at said bonded interface, said thermal treatment selected from the group consisting of furnace anneal and/or rapid thermal anneal (RTA).

22. The method of claim 21 wherein said step of annealing includes an anneal ambient selected from the group consisting of air, N_2 and Ar.

23. The method of claim 21 wherein said step of annealing includes the step of heating to a temperature in the range from about 100°C to about 800°C.

24. The method of claim 5 wherein a highly selectively wet etching process is used to remove Si substrate of said first substrate.

25. The method of claim 24 wherein EPPW, KOH or TMAH is used as the wet etchant.

26. The method of claim 24 wherein the wet etching in EPPW, KOH or TMAH is at a temperature in the range from about 70°C to about 120°C.

27. The method of claim 24 wherein said step of Chemo-Mechanical Polishing (CMP) includes removing said step-graded $Si_{1-x}Ge_x$ layer and to polish the exposed $Si_{1-y}Ge_y$ relaxed to provide a smoothness in the range from about 0.3nm to about 1nm.

28. The method of claim 24 wherein a relaxed $Si_{1-y}Ge_y$ layer may be epitaxially grown on said top surface of said smoothed relaxed $Si_{1-y}Ge_y$ layer.

29. The method of claim 26 wherein said step of epitaxially growing said relaxed $Si_{1-y}Ge_y$ layer includes growing to a thickness in the range from about 50nm to about 500nm.

30. The method of claim 24 further including the step of growing one of strained Si or strained SiGe or deposition of a n+ Poly Si layer on said smoothed relaxed $Si_{1-y}Ge_y$ layer.

31. A multi layer substrate for use in forming integrated circuits comprising:
a silicon containing substrate,
a silicon oxide layer on said silicon containing substrate, and a relaxed $Si_{1-y}Ge_y$ layer on said silicon oxide layer.

32. The multi layer substrate of claim 31 wherein said silicon oxide layer has a buried upper surface roughness in the range from about 0.3 nm to about 1 nm RMS.

33. The multi layer substrate of claim 31 wherein said relaxed $Si_{1-y}Ge_y$ layer has a buried lower surface roughness in the range from about 0.3 nm to about 1 nm RMS.

34. The multi layer substrate of claim 31 wherein said silicon oxide layer and said relaxed $Si_{1-y}Ge_y$ layer are chemically bonded together.

35. The multilayer substrate of claim 34 wherein said silicon oxide layer bonded to said relaxed $Si_{1-y}Ge_y$ layer has a buried surface roughness in the range from about 0.3 nm to about 1 nm RMS.

36. The multi layer substrate of claim 31 wherein said relaxed $Si_{1-y}Ge_y$ layer has a value y in the range from about 0.2 to about 0.5.

37. The multi layer substrate of claim 31 further including a strained epitaxial silicon containing layer on said relaxed $Si_{1-y}Ge_y$ layer.

38. A multi layer substrate for use in forming integrated circuits comprising:
a silicon substrate, and
a relaxed $Si_{1-y}Ge_y$ layer on said silicon substrate, said relaxed $Si_{1-y}Ge_y$ layer chemically bonded to said silicon substrate.

39. The multi layer substrate of claim 38 wherein said relaxed $Si_{1-y}Ge_y$ layer has a buried lower surface roughness in the range from about 0.3 nm to about 1 nm RMS.

40. The multi layer substrate of claim 38 wherein said silicon substrate bonded to said relaxed $Si_{1-y}Ge_y$ layer has a buried surface roughness in the range from about 0.3 nm to about 1 nm RMS.

41. The multi layer substrate of claim 38 wherein said relaxed $Si_{1-y}Ge_y$ layer has a value y in the range from about 0.2 to about 0.5.

42. The multi layer substrate of claim 38 further including a strained epitaxial silicon containing layer on said relaxed $Si_{1-y}Ge_y$ layer.